AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (original) A peripheral bus switch comprising:

a virtual peripheral bus;

a first bridge operably coupled on a first side to the virtual peripheral bus and that supports connection on a second side to a peripheral bus fabric;

a second bridge operably coupled on a first side to the virtual peripheral bus and that supports connection on a second side to the peripheral bus fabric; and

a configurable host bridge operably coupled to the virtual peripheral bus, wherein the configurable host bridge supports a host mode of operation in which it serves as a host bridge, and wherein the configurable host bridge supports a device mode of operation in which it operates as a device.

2. (original) The peripheral bus switch of claim 1, wherein in the host mode of operation the configurable host bridge configures devices of the peripheral bus fabric.

3. (original) The peripheral bus switch of claim 1, wherein in the host mode of operation the configurable host bridge serves as a root bridge of the peripheral bus fabric.

4. (original) The peripheral bus switch of claim 1, wherein in the host mode of operation the virtual peripheral bus serves as a root bus of the peripheral bus fabric.

5. (original) The peripheral bus switch of claim 1, wherein in the device mode of operation:

a root host bridge configures the peripheral bus fabric; and

the configurable host bridge appears to be a peripheral bus device.

6. (original) The peripheral bus switch of claim 5, wherein in the device mode of operation the virtual peripheral bus appears to be a peripheral bus of the peripheral bus fabric.

7. (original) The peripheral bus switch of claim 6, wherein in the device mode of operation the virtual peripheral bus appears to the root host bridge to be a Peripheral Component Interconnect (PCI) bus, a PCI-X bus, a PCI Express bus, or a Hyper Transport bus of the peripheral bus fabric.

8. (original) The peripheral bus switch of claim 1, wherein the virtual peripheral bus, the first bridge, the second bridge, and the configurable host bridge coupled to the virtual peripheral bus are emulated by a system on a chip comprising:

at least one processing unit;

memory;

an internal bus operably coupled to the at least one processing unit and the memory;

a plurality of input ports operably coupled to the internal bus that receive peripheral bus transactions; and

a plurality of output ports operably coupled to the internal bus that transmit peripheral bus transactions.

9. (original) The peripheral bus switch of claim 1, wherein the configurable host bridge shares a memory space with at least one other host bridge coupled via the peripheral bus fabric.

10. (original) The peripheral bus switch of claim 1, wherein:

at least a portion of the peripheral bus fabric supports at least one version of the HyperTransport™ specification; and

the virtual peripheral bus appears to support one or more versions of the Peripheral Component Interconnect (PCI) specification, the PCI-X specification, or the PCI Express specification.

11-27. (canceled)